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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/777,157

02/13/2004

Shuji Mayama

118680

4034

25944

7590

11/15/2005

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EXAMINER

ENGLUND, TERRY LEE

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/777,157	<b>Applicant(s)</b> MAYAMA ET AL.	
	<b>Examiner</b> Terry L. Englund	<b>Art Unit</b> 2816	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 29 August 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 7-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 7-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 August 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment/Drawings***

The amendment and drawings submitted on Aug 29, 2005 were reviewed and considered with the following results:

The drawing changes overcame the objections to Figs. 2, 4, and 5 as described in the previous Office Action. Therefore, those changes have been approved, and the drawing objections have been withdrawn.

The amended paragraphs overcame the objections to the disclosure, which have also been withdrawn.

Cancelled claims 5-6 overcame their rejections under 35 U.S.C. 103(a), with respect to Nadd/Vajdic et al., moot.

Amended claim 1 did not satisfactorily overcome its rejection under 35 U.S.C. 112 as described in the previous Office Action, and some of the amended changes created new problems. Therefore, these rejections are described later under the appropriate section.

Amended claim 2 overcame its rejection under 35 U.S.C. 112, which has now been withdrawn.

Amended claim 1 overcame the rejections of claims 1-4 under 35 U.S.C. 103(a), with respect to Nadd/Ito et al. Therefore, those rejections have been withdrawn because the Ito et al. reference will not have the second resistor connected to the first diode as now recited within claim 1. However, modified claim rejections under 35 U.S.C. 103(a) are described later, taking into account the amended changes.

Newly added claims 7-9 are also rejected, and their respective rejections are described later under the appropriate section.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, and 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear in claim 1 how the first/second follower circuits actually relate to the first/second switches. For example, can the follower circuits and switches be distinct, separate elements, or must each switch be a part of a corresponding follower circuit, or vice versa? As presently written, lines 24-30 of claim 1 are misleading since the recited limitations imply that each of the first and second follower circuits comprises its own respective first/second transistors, and first/second resistors. However, doesn't each follower circuit actually comprise only one transistor and one resistor?

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are how any of the third-fifth resistors, and the third diode, of claim 7 relates to any of the other elements already recited within claim 1. As presently written, the only thing they have in common is their being in the charge pump circuit.

Claim 8 recites the limitation "the fourth resistor and the third diode" in line 2. There is insufficient antecedent basis for this limitation in the claim. Also, the use of "the fourth resistor" implies a third resistor that is not recited within the claim's chain of dependency.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

***Claim Rejections - 35 USC § 103***

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadd; a reference cited in the previous Office Action, in view of Pierce et al. (Pierce), another reference cited in the previous Office Action. Fig. 2 of Nadd shows a charge pump circuit comprising first/second diodes 45/46 interposed in series between input portion 49 receiving power source input Vcc and an output portion (i.e. the cathode of diode 46 coupled to the gate of FET 32) for outputting a stepped up voltage, wherein the forward direction of each diode is directed to the

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output portion side; capacitor 44 is interposed between a connecting portion (i.e. cathode) of first diode 45 on the side of the output portion, and ground (via the understood pull-down section of buffer 42); and driver 41 provides a clock signal which allows alternate/opposite phase type (e.g. complementary) operation of buffer 42. Nadd discloses the charge pump “can be of any desired type” on line 25 of column 4, and that high side switching circuits can be used in automotive applications (e.g. see column 3, line 19-22). However, although Nadd shows buffer 42 (that one of ordinary skill in the art would recognize as one type of a pull-up/pull-down circuit), the reference does not clearly show or disclose the first/second switches, and a constant current charging and discharging circuit with first/second follower circuits, wherein each follower circuit comprises at least one transistor and a corresponding resistor. Fig. 2C of Pierce shows one type of a pull-up/pull-down circuit with a respect to resistors 223 and 225, and inverter 224. This circuit is effectively a constant current charging and discharging circuit in that it continuously provides some type of current to its output (e.g. see column 2, lines 8-19). It would have been obvious to one of ordinary skill in the art to replace Nadd’s (generic - no details) buffer 42 with Pierce’s pull-up/pull-down type circuit, one known type of buffer. With this configuration, first switch 224b will conduct and cutoff a connecting path between connecting portion 43 of Nadd’s capacitor 44 and ground; and second switch 224a will conduct and cutoff a connecting path between connecting portion 43 and Nadd’s input portion 49. The first/second switches will conduct alternately in phases opposite to each other with respect to the signal received from driver 41. Pierce’s circuit can be deemed one type of constant current charging and discharging circuit, since it would continuously allow some current to flow to connecting portion 43 of capacitor 44. Since the output follows the input in an inverse manner, Pierce’s 224b/225 and

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223/224a can be considered first/second follower circuits. When first switch 224b of first follower circuit 225/224b conducts, a current from input portion 49 flows to ground, thus charging capacitor 44 via Nadd's 45, and Pierce's 224b/225. When second switch 224a of second follower circuit 223/224a conducts, a current from input portion 49 flows to second diode 46, thus allowing capacitor 44 to discharge. As shown in Pierce's Fig. 2C, first follower 225/224b has first transistor 224b coupled between connection portion 226 (corresponding to 43 of Nadd's capacitor 44) and first resistor 225, wherein first resistor 225 is coupled between the first transistor and ground, thus being arranged along a first path. Second follower 223/224a has second transistor 224a coupled between the connection portion and second resistor 223, wherein second resistor 223 is coupled between the second transistor and input portion 49, thus being arranged along a second path. Since input portion 49 is connected to the anode of first diode 45, second resistor 223 is also connected to the first diode. Each combination of transistor and resistor is connected in series to a respective upstream side, or a downstream side, in a current flowing direction with respect to the transistor. Therefore, claims 1-2 are rendered obvious. With first resistor 225 connected between first transistor 224b and ground, claim 9 is also rendered obvious. The use of Pierce's buffer will provide Nadd's circuit with a means to minimize bouncing in the power supply voltage (e.g. Vcc), and in the ground supply voltage, during switching (e.g. from when 224a is completely on and 224b is completely off, to when 224a is completely off, and 224b is completely on). Fig. 2 of Nadd shows the output of charge pump circuit 40 being used to drive a gate of FET 32; column 1, lines 11-16 discloses that the gate of a MOS requires a higher potential than the power supply; and column 3, lines 19-22 clearly discloses high side switching circuits can be used in automotive applications. Therefore,

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claims 3-4 are rendered obvious with respect to the use of the Nadd/Pierce charge pump circuit with vehicle mounting, and for driving the gate of a FET. For example, Nadd's FET 32 is driven by charge pump circuit 40, and it controls power source current supplied from power source line Vcc to load 31.

Claims 1-4, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadd, a reference cited in the previous Office Action, in view of Ebihara, a reference found during a recent update search. Fig. 2 of Nadd shows charge pump circuit 40 comprising first/second diodes 45/46 interposed in series between input portion 49 receiving power source input Vcc and an output portion (i.e. the cathode of diode 46 coupled to the gate of FET 32) for outputting a stepped up voltage, wherein the forward direction of each diode is directed to the output portion side; capacitor 44 is interposed between a connecting portion (i.e. cathode) of first diode 45 on the side of the output portion, and ground (via the understood pull-down section of buffer 42); and driver 41 provides a clock signal which allows alternate/opposite phase type (e.g. complementary) operation of buffer 42. Nadd discloses the charge pump "can be of any desired type" on line 25 of column 4, and that high side switching circuits can be used in automotive applications (e.g. see column 3, line 19-22). However, although Nadd shows buffer 42 (that one of ordinary skill in the art would recognize as one type of a pull-up/pull-down circuit), the reference does not clearly show or disclose the first/second switches, and a constant current charging and discharging circuit with first/second follower circuits, wherein each follower circuit comprises at least one transistor and a corresponding resistor. Ebihara's Fig. 12 shows one type of a pull-up/pull-down circuit (e.g. one type of buffer) 160. This circuit is considered one type of a constant current charging and discharging circuit because its complementary type operation of



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transistors 104 and 111 will continuously provide some type of current to its output. Therefore, it would have been obvious to one of ordinary skill in the art to replace Nadd's (generic - no details) buffer 42 with Ebihara's pull-up/pull-down type circuit 160. With this configuration, first switch 111 will conduct and cutoff a connecting path between connecting portion 43 of capacitor 44 and ground (e.g. low voltage L1 of Ebihara); and second switch 104 will conduct and cutoff a connecting path between connecting portion 43 and input portion 49 (e.g. high voltage H1 of Ebihara). The first/second switches will conduct alternately in phases opposite to each other with respect to the signal received from driver 41 (which can be used instead of Ebihara's driver 999). Ebihara's circuit can be deemed one type of constant current charging and discharging circuit, since it would continuously allow some current to flow to connecting portion 43 of capacitor 44. Since the output effectively follows the input, 111/113 and 104/106 of Ebihara can be considered first/second follower type circuits, respectively. When first switch 111 of first follower circuit 111/113 conducts, a current from input portion 49 flows to ground, thus charging capacitor 44 via Nadd's 45, and Ebihara's 111/113. When second switch 104 of second follower circuit 104/106 conducts, a current from input portion 49 flows to second diode 46, thus allowing capacitor 44 to discharge. As shown in Fig. 12 of Ebihara, first follower 111/113 has first transistor 111 coupled between a connection portion (corresponding to 43 of Nadd's capacitor 44) and first resistor 113, wherein first resistor 113 is coupled between the first transistor and ground, thus being arranged along a first path. Second follower 104/106 has second transistor 104 coupled between the connection portion and second resistor 106, wherein second resistor 106 is coupled between the second transistor and input portion 49, thus being arranged along a second path. Since input portion 49 is connected to the anode of first diode 45, second resistor

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106 is also connected to the first diode. Each combination of transistor and resistor is connected in series to a respective upstream side, or a downstream side, in a current flowing direction with respect to the transistor. Therefore, claims 1-2 are rendered obvious. With first resistor 113 connected between first transistor 111 and ground, claim 9 is also rendered obvious. The use of Ebihara's buffer will provide Nadd's circuit with a means to help maintain the power source lines (i.e. Vcc and ground of Nadd) stabilized (e.g. see column 10, lines 10-14) during switching (e.g. from when 104 is completely on and 111 is completely off, to when 104 is completely off, and 111 is completely on). Fig. 2 of Nadd shows the output of charge pump circuit 40 being used to drive a gate of FET 32; column 1, lines 11-16 discloses that the gate of a MOS requires a higher potential than the power supply; and column 3, lines 19-22 clearly discloses high side switching circuits can be used in automotive applications. Therefore, claims 3-4 are rendered obvious with respect to the use of the Nadd/Ebihara charge pump circuit with vehicle mounting, and for driving the gate of a FET. For example, Nadd's FET 32 is driven by charge pump circuit 40, and it controls power source current supplied from power source line Vcc to load 31. The buffer of Ebihara also shows third resistor 105, fifth resistor 102, fourth resistor 109, and third diode 108 coupled in series (e.g. between H1 and the base of 111), rendering claim 7 obvious. A first connecting point between fourth resistor 109 and third diode 108 is connected to the base of first transistor 111, via diode 108. Therefore, claim 8 is also rendered obvious.

No claim is allowable.

Claims 5-6 have been cancelled.

**THIS ACTION IS MADE FINAL.** The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

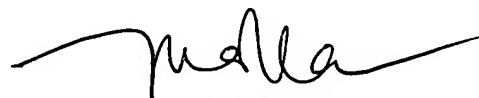
The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Terry L. Englund  
2 November 2005



TUAN T. LAM  
PRIMARY EXAMINER

**Amendments to the Drawings:**

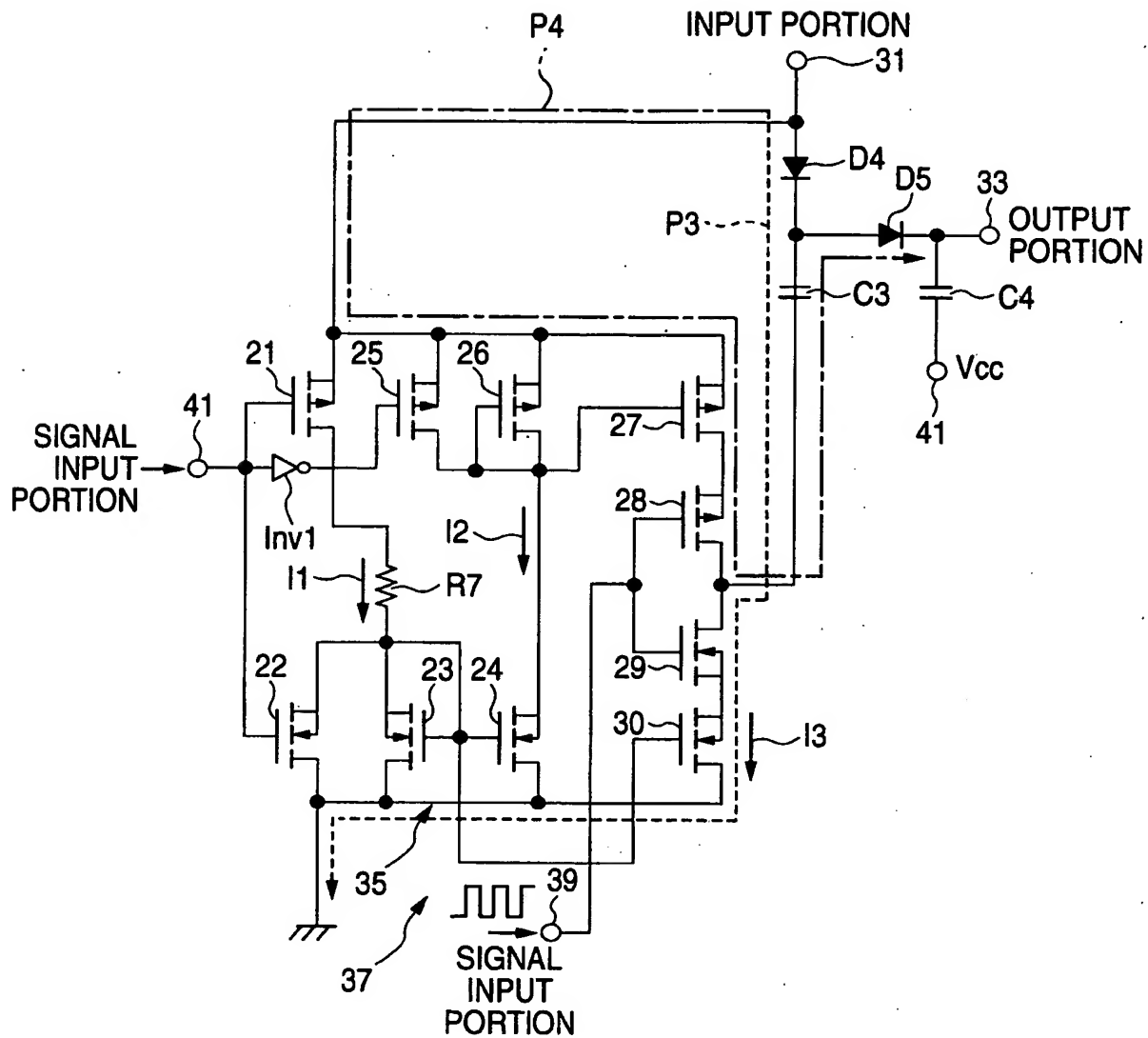
The attached replacement drawing sheets makes changes to Figs. 2, 4 and 5 and replace the original sheets with Figs. 2, 4 and 5.

Attachment: Replacement Sheets

Approved  
11.2.05  
TLE

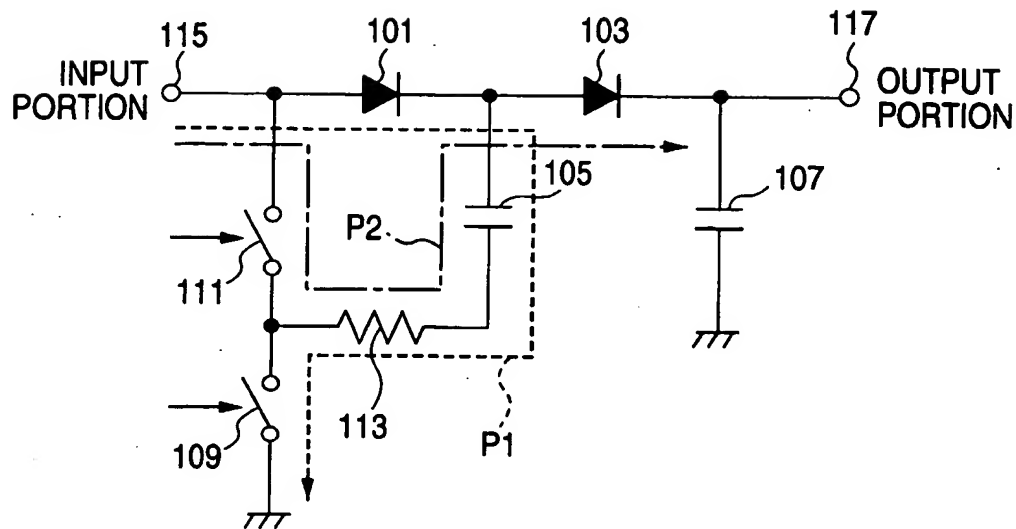


FIG. 2



**FIG. 4**

Prior Art

**FIG. 5**

Prior Art

